

What is claimed is:

1. An electrical device, comprising:
 - an integrated circuit supported by a base layer and having a plurality of integrated circuit devices, wherein at least one of the plurality of integrated circuit devices has a semiconductor structure formed by a method comprising:
 - forming an insulator layer on a base layer, wherein the insulator layer has a surface;
 - patterning the insulator layer to define a hole, wherein the hole has sidewalls defined by the insulator layer and a bottom defined by an exposed portion of the base layer;
 - forming at least one titanium-containing layer overlying the surface of the insulator layer and the sidewalls and the bottom of the hole by chemical vapor deposition;
 - forming a plug layer overlying the titanium-containing layer and filling the hole; and
 - removing a portion of the plug layer overlying the surface of the insulator layer subsequent to removing the portion of the plug layer by exposing the portion of the titanium-containing layer to a sulfuric acid solution.
2. The device of claim 1, wherein the integrated circuit is adapted for use in a semiconductor die.
3. The device of claim 2, wherein the titanium-containing layer includes a titanium layer and a titanium nitride layer overlying the titanium layer.
4. The device of claim 3, wherein the plug layer includes tungsten.

5. The device of claim 1, wherein the titanium-containing layer includes a titanium layer and a titanium nitride layer overlying the titanium layer.
6. The device of claim 5, wherein the plug layer includes a tungsten layer.
7. The device of claim 1, wherein the plug layer includes a tungsten layer.
8. The device of claim 1, wherein the integrated circuit includes a memory device having an array of memory cells.
9. The device of claim 8, wherein the memory device further includes:
 - a row access circuit coupled to the array of memory cells;
 - a column access circuit coupled to the array of memory cells; and
 - an address decoder circuit coupled to the row access circuit and the column access circuit.
10. The device of claim 9, wherein the titanium-containing layer includes a titanium layer and a titanium nitride layer overlying the titanium layer.
11. The device of claim 10, wherein the plug layer includes a tungsten layer.
12. The device of claim 1, wherein the integrated circuit includes a memory module that comprises:
 - a support;
 - a plurality of leads extending from the support;
 - a command link coupled to at least one of the plurality of leads;
 - a plurality of data links, wherein each data link is coupled to at least one of the plurality of leads; and

at least one memory device contained on the support and coupled to the command link, wherein the at least one memory device includes an array of memory cells, wherein at least one memory cell of the array of memory cells has a bit-line contact.

13. The device of claim 12, wherein the at least one memory device includes:
a row access circuit coupled to the array of memory cells;
a column access circuit coupled to the array of memory cells; and
an address decoder circuit coupled to the row access circuit and the column access circuit.

14. The device of claim 12, wherein the titanium-containing layer includes a titanium layer and a titanium nitride layer overlying the titanium layer.

15. The device of claim 14, wherein the plug layer includes a tungsten layer.

16. The device of claim 1, wherein the integrated circuit includes a memory system, comprising:

a controller;
a command link coupled to the controller;
a data link coupled to the controller; and
a memory device coupled to the command link and the data link, wherein the memory device comprises an array of memory cells, wherein at least one memory cell has a bit-line contact

17. The device of claim 16, wherein the at least one memory device includes:
a row access circuit coupled to the array of memory cells;
a column access circuit coupled to the array of memory cells; and

an address decoder circuit coupled to the row access circuit and the column access circuit.

18. The device of claim 16, wherein the titanium-containing layer includes a titanium layer and a titanium nitride layer overlying the titanium layer.

19. The device of claim 18, wherein the plug layer includes a tungsten layer.

20. The device of claim 1, wherein the integrated circuit includes a semiconductor die adapted to connect to an electronic system.

21. The device of claim 20, wherein the titanium-containing layer includes a titanium layer and a titanium nitride layer overlying the titanium layer.

22. The device of claim 21, wherein the plug layer includes a tungsten layer.

23. The device of claim 1, wherein the integrated circuit includes a semiconductor die adapted to connect to a circuit module that includes a plurality of leads connected to a processor.

24. The device of claim 1, wherein the integrated circuit is supported by a base layer and having a plurality of integrated circuit devices.